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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/762,627	01/23/2004	Raminda U. Madurawe		5016

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EXAMINER	
PHAM, LONG	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 06/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/762,627	MADURAWE, RAMINDA U.	
	Examiner	Art Unit	
	Long Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-12,14-16 and 18-20* is/are rejected.

7)☒ Claim(s) *1-6,13 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2 IDS'*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

In claim 1, the "said channel height", "said first insulator layer", "said thin film properties", "said gate insulator properties", "said gate material properties", " the gate insulator surface", and "said channel resistance" do not have antecedent bases. Also, see claims 13 and 17 for the same problems.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-6, 13, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Ichimori et al. (US publication 2002/0036320) in combination with Vinal (US patent 5,151,759) and Houston (US publication 2002/0180069).

With respect to claims 1, 13, and 17, Ichimori et al. teach a method of fabricating a semiconductor insulated-gate field effect transistor (Gated-FET) (see figs. 1 and associated text):

depositing a semiconductor thin film layer 16 on a first thick insulator 51; and

forming a substantially rectungular channel region 16 in said semiconductor thin film layer, wherein the height of the channel region comprising the entire thin film thickness; and

depositing a gate insulator layer above said channel region; and

depositing a gate material 13 above said gate insulator layer, said material forming a gate region above said channel region.

Ichimori et al. fail to teach doping the channel region and optimizing the thin film layer, gate insulator, and gate material by providing the gate region with a first voltage level that modulates channel resistance to a substantially non-conductive state by fully depleting majority carriers from the channel region and a second voltage level that modulates channel resistance to a substantial conductive state by at least partially accumulating majority carriers near a surface of the gate insulator layer,

Vinal teaches a method of fabricating a Gated-FET device comprises of doping the channel region 15 and optimizing the thin film layer, gate insulator, and gate material by providing the gate region with a first voltage level that modulates channel resistance to a substantially non-conductive state by fully depleting majority carriers from the channel region 15 and a second voltage level that modulates channel resistance to a substantial conductive state by at least partially accumulating majority carriers in the channel region 15. See fig. 23 and col. 36, lines 56-61 and figs. 24-25 and col. 36, line 65 to col. 37, line 10.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the above teachings of Vinal into the process of Ichimori et al. to maximize the carrier mobility and minimize the hot electron effect. See the abstract.

With respect to claim 2, Ichimori et al. further teach the semiconductor thin film layer is made of silicon. See [0028[.

With respect to claim 3, the use of oxide as gate insulator material and SOI material is well-known.

With respect to claim 4, the use of doped polysilicon or metal as gate material is well-known.

With respect to claim 5, Ichimori et al. fail to teach selecting high work function material for the gate region when the device is p channel or p doped channel and low work function material for the gate region when the device is n channel or n doped channel.

Houston teaches choosing high work function material for the gate region when the device is p channel or p doped channel and low work function material for the gate region when the device is n channel or n doped channel to provide higher threshold voltage. See [0023].

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the above teachings of Houston into the process of Ichimori et al. and Vinal to obtain the benefit of higher threshold voltage.

With respect to claim 6, the doping of source and drain to a higher level than the channel region is well-known in the art.

Further with respect claim 6, the use of same dopant type for the channel and source and drain is well-known.

Further with respect claim 6, a conducting path comprising the entire thickness of the thin film layer would inherently be formed between the source and drain and through the channel region in the process of Ichimori et al.

Further with respect to claims 13 and 17, Ichimori et al. further teach forming source and drain on opposite sides of the channel region in the thin film layer.

Further with respect to claims 13 and 17, the heavily doping of source and drain with n or p type dopant is well-known.

Further with respect to claims 13 and 17, use of heavily p or n doped polysilicon gate is well-known.

Further with respect to claims 13 and 17, the source and drain would inherently be disconnected when the channel region is in non-conductive state and would inherently be connected the channel region is in conductive state.

Allowable Subject Matter

4. Claims 7-12 and 14-16 and 18-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 571-272-1714. The examiner can normally be reached on M-F, 7:30AM-3:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Long Pham
Primary Examiner
Art Unit 2814

LP